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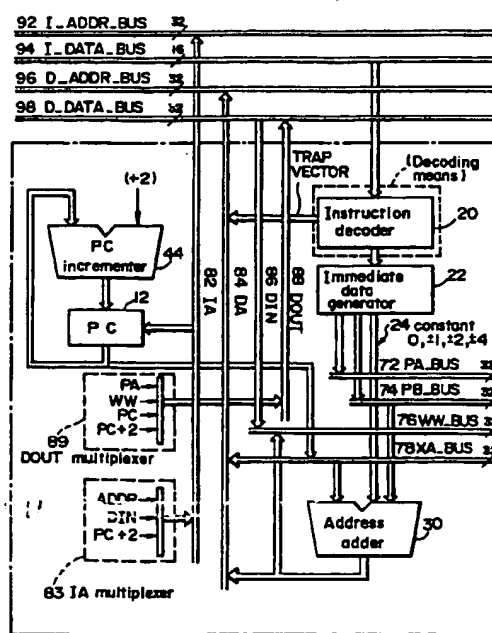
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(54) **Data processing circuit, microcomputer, and electronic equipment**

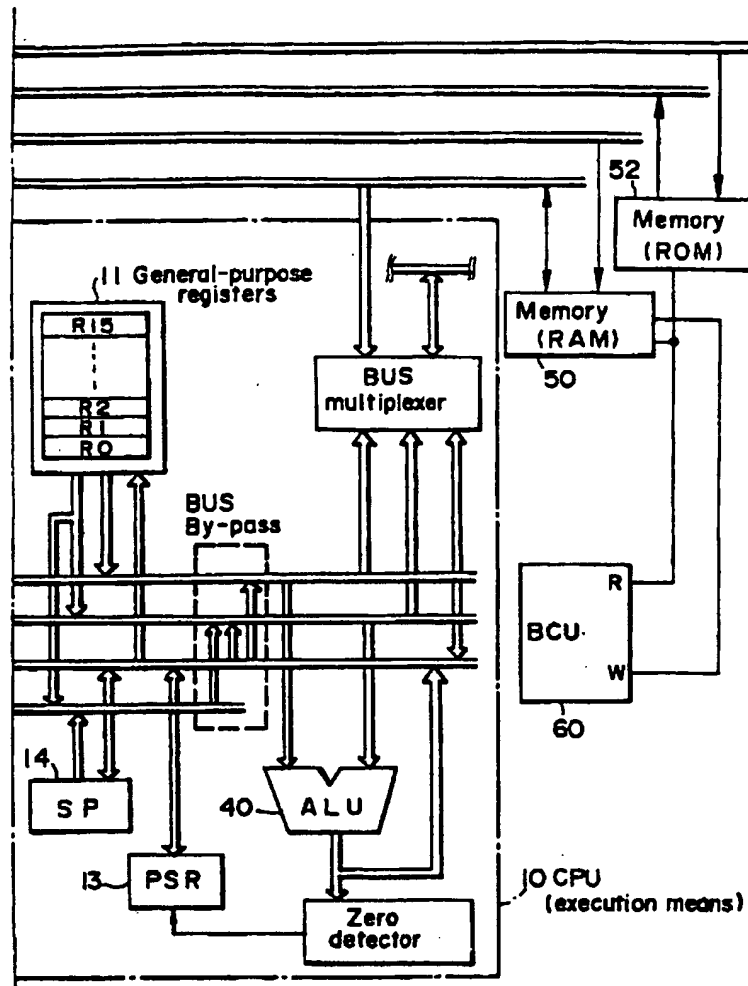
(57) The data processing circuit of this invention enables efficient description and execution of processes that act upon the stack pointer, using short instructions. It also enables efficient description of processes that save and restore the contents of registers, increasing the speed of processing of interrupts and subroutine calls and returns. A CPU that uses this data processing circuit comprises a dedicated stack pointer register SP and uses an instruction decoder to decode a group of dedicated stack pointer instructions that specify the SP as an implicit operand. This group of dedicated stack pointer instructions are implemented in hardware by using general-purpose registers, the PC, the SP, an address adder, an ALU, a PC incrementer, internal buses, internal signal lines, and external buses. This group of dedicated stack pointer instructions comprises SP-relative load instructions, stack pointer move instructions, a call instruction, a ret instruction, a sequential push instruction, and a sequential pop instruction.

FIG. 1A



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FIG. 1B





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| The present search report has been drawn up for all claims | | | |
| Place of search THE HAGUE | | Date of completion of the search 12 November 1998 | Examiner Daskalakis, T |
| CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document | | T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document | |

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